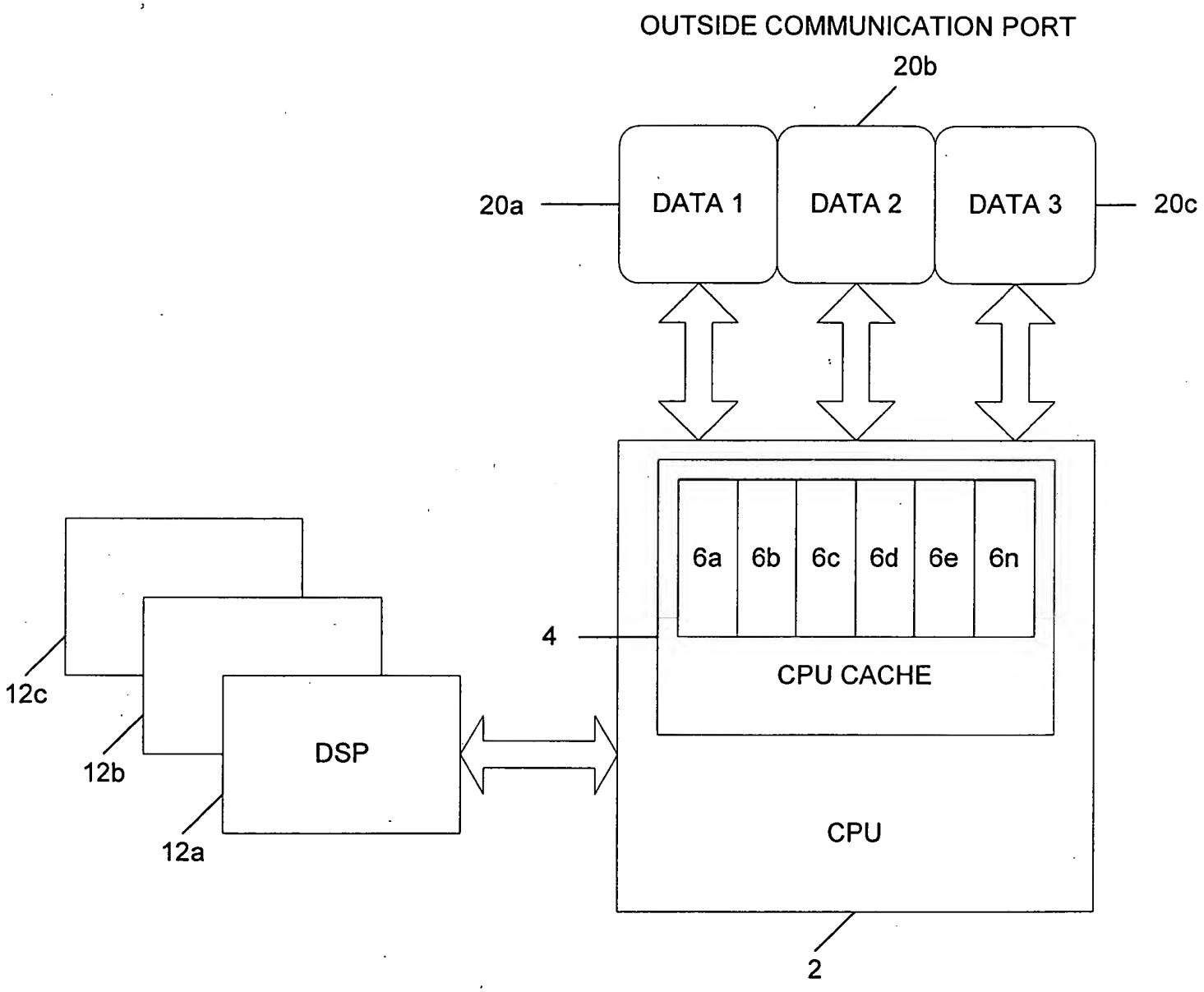



FIG. 1 (PRIOR ART)

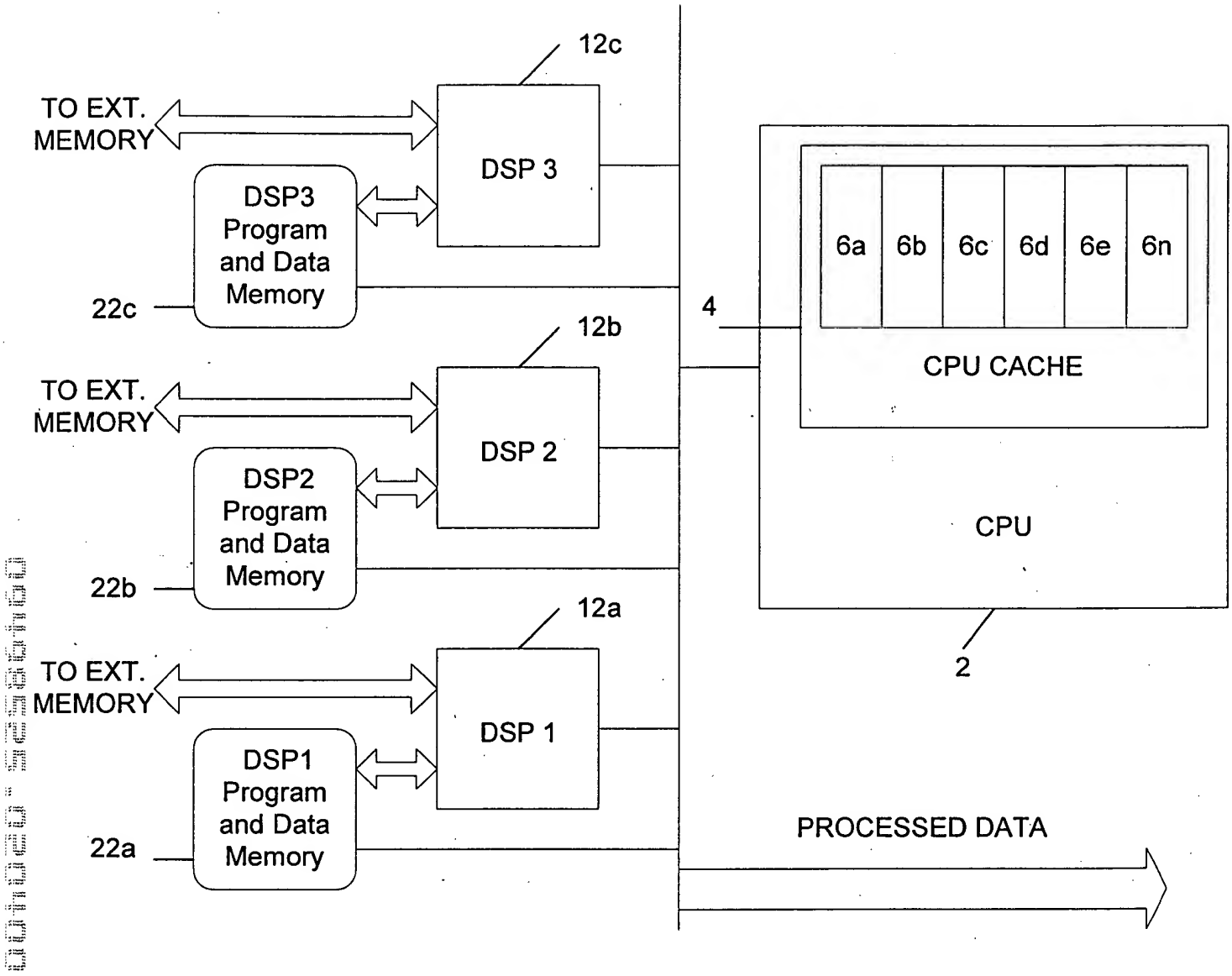



FIG. 2 (PRIOR ART)

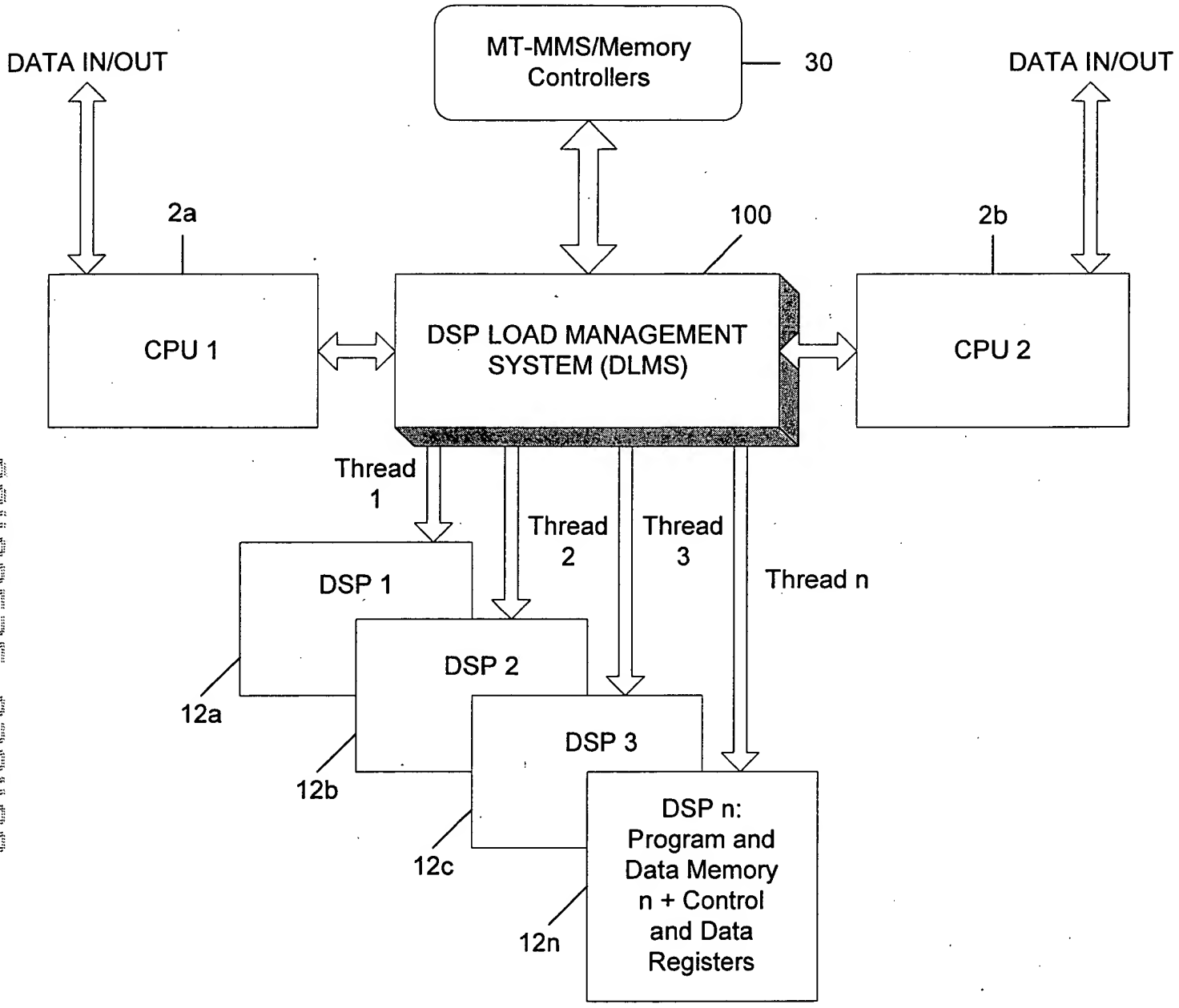

DATA IN/OUT
MT-MMS/Memory Controllers
30
DATA IN/OUT
2a
100
2b
CPU 1
DSP LOAD MANAGEMENT SYSTEM (DLMS)
CPU 2
Thread 1
Thread 2
Thread 3
Thread n
DSP 1
DSP 2
DSP 3
12a
12b
12c
12n
DSP n: Program and Data Memory n + Control and Data Registers

FIG. 3A

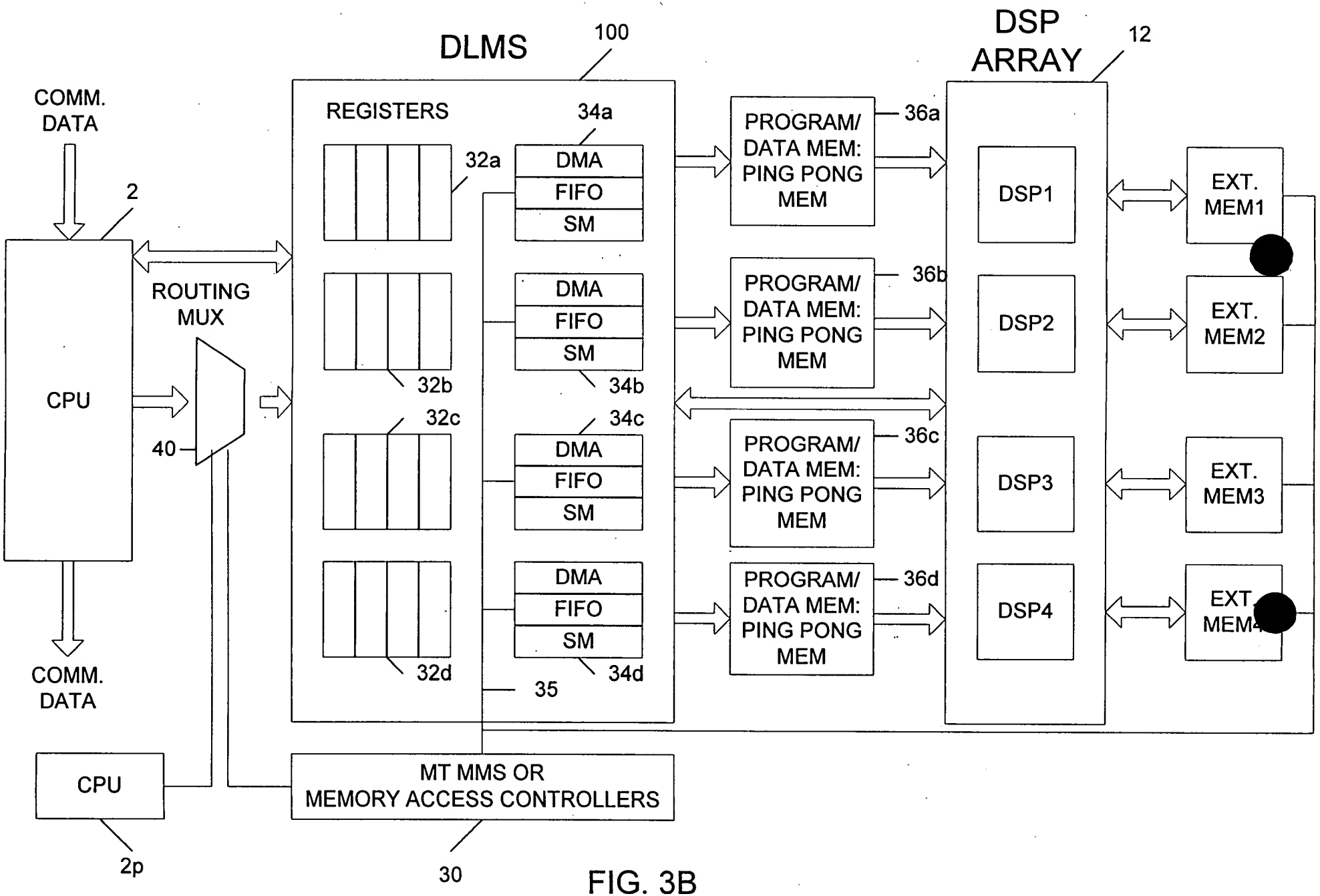
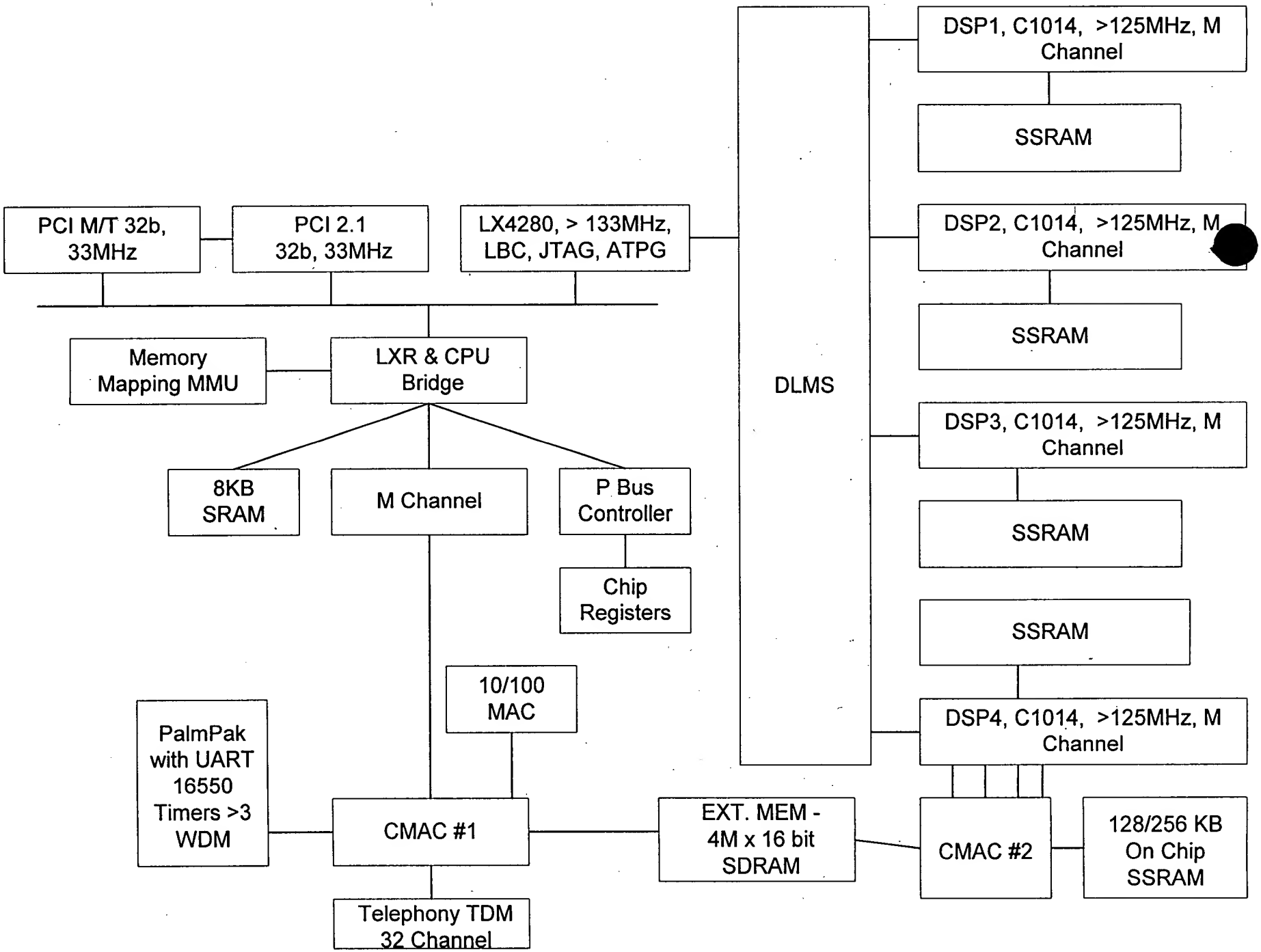

DLMS
100
DSP ARRAY
12
COMM. DATA
2
REGISTERS
34a
32a
DMA
FIFO
SM
PROGRAM/ DATA MEM: PING PONG MEM
36a
DSP1
EXT. MEM1
ROUTING MUX
CPU
32b
34b
36b
DSP2
EXT. MEM2
40
32c
34c
36c
DSP3
EXT. MEM3
32d
34d
36d
DSP4
EXT. MEM4
35
COMM. DATA
CPU
MT MMS OR MEMORY ACCESS CONTROLLERS
2p
30

FIG. 3B

FIG. 3C


PCI M/T 32b, 33MHz
PCI 2.1 32b, 33MHz
LX4280, > 133MHz, LBC, JTAG, ATPG
Memory Mapping MMU
LXR & CPU Bridge
8KB SRAM
M Channel
P Bus Controller
Chip Registers
10/100 MAC
PalmPak with UART 16550 Timers >3 WDM
CMAC #1
Telephony TDM 32 Channel
DLMS
EXT. MEM - 4M x 16 bit SDRAM
DSP1, C1014, >125MHz, M Channel
SSRAM
DSP2, C1014, >125MHz, M Channel
SSRAM
DSP3, C1014, >125MHz, M Channel
SSRAM
SSRAM
DSP4, C1014, >125MHz, M Channel
CMAC #2
128/256 KB On Chip SSRAM

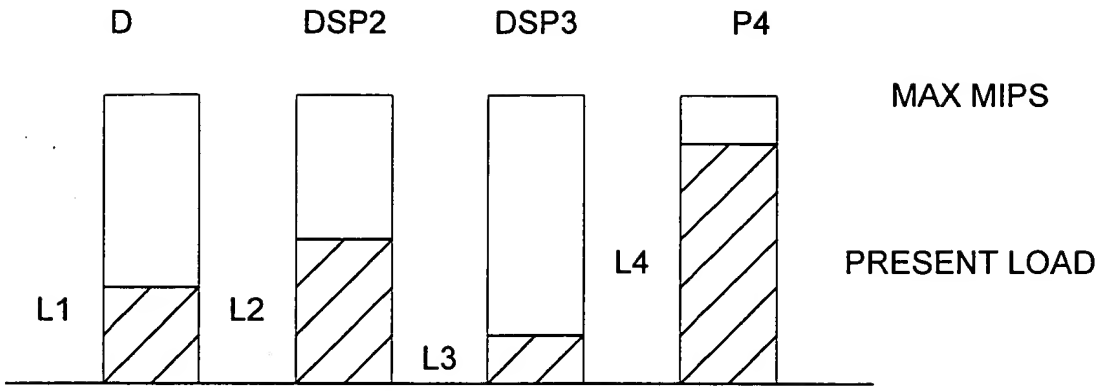



FIG. 4A

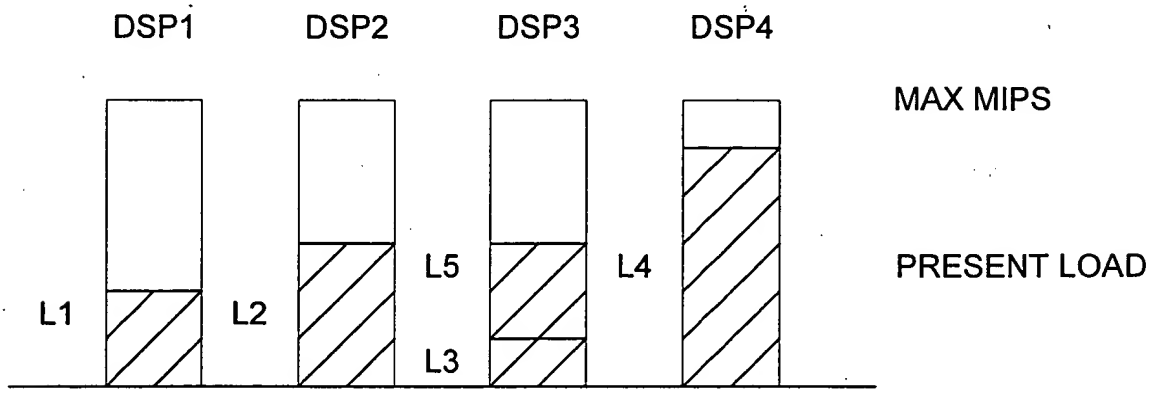



FIG. 4B

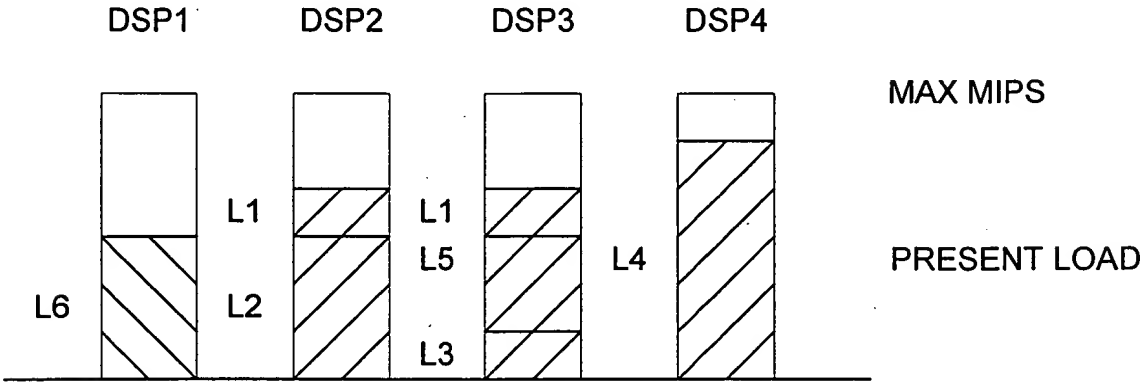



FIG. 4C

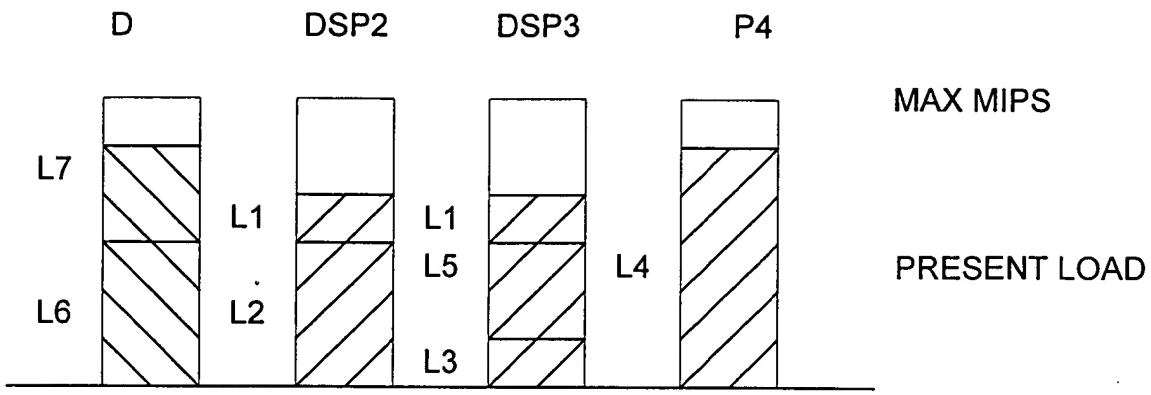



FIG. 4D

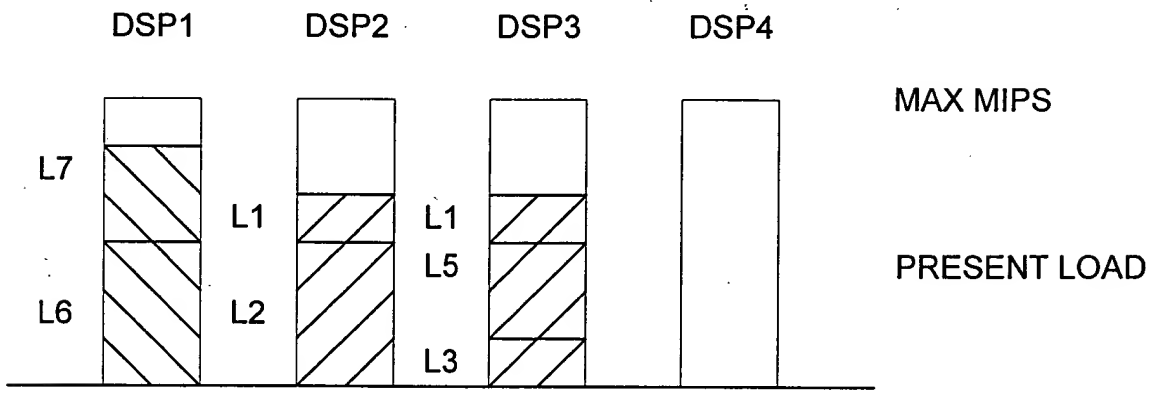



FIG. 4E

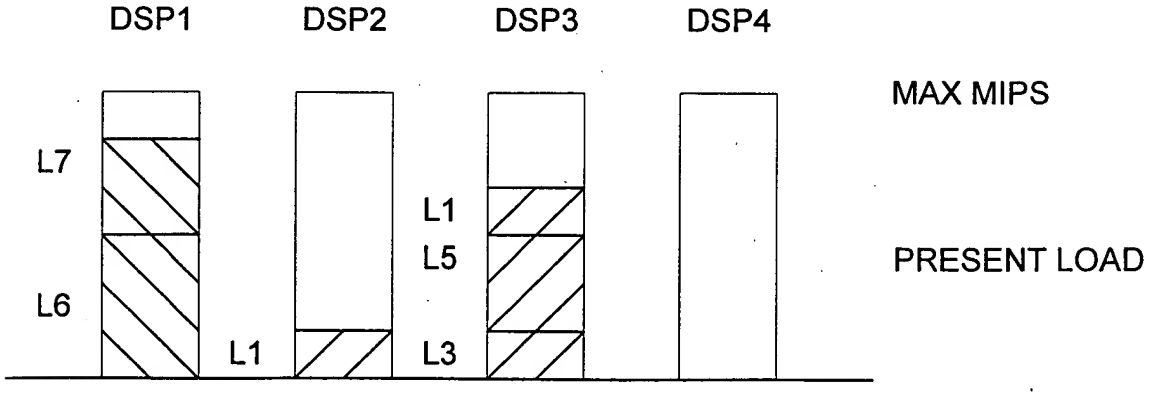



FIG. 4F

| | DSP1 | DSP2 | DSP3 | |
|---|---|---|---|---|
| ALGORITHM 1 | 15 | | | |
| ALGORITHM 2 | | 5 | | |
| ALGORITHM 3 | | | 2 | |
| ALGORITHM 4 | | | 2 | |

FIG. 4G

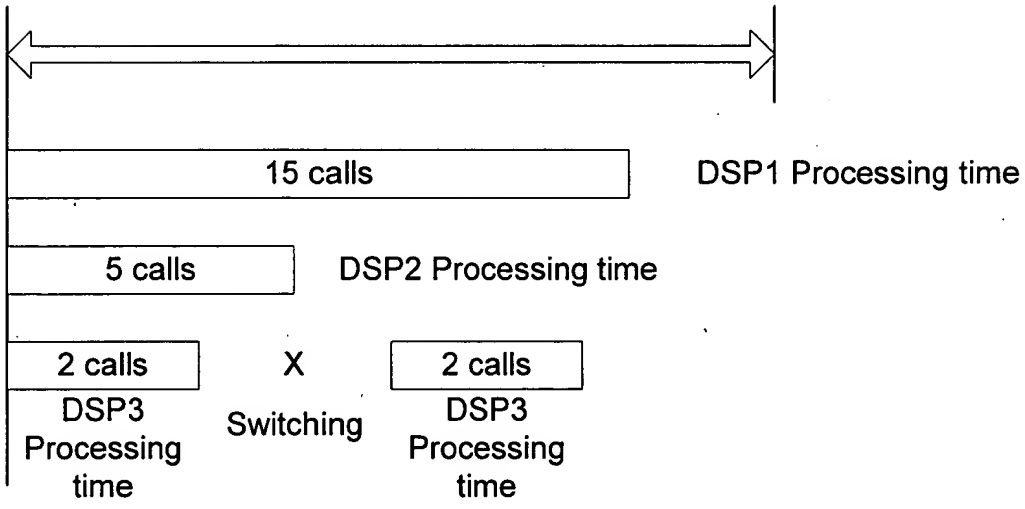



FIG. 4H

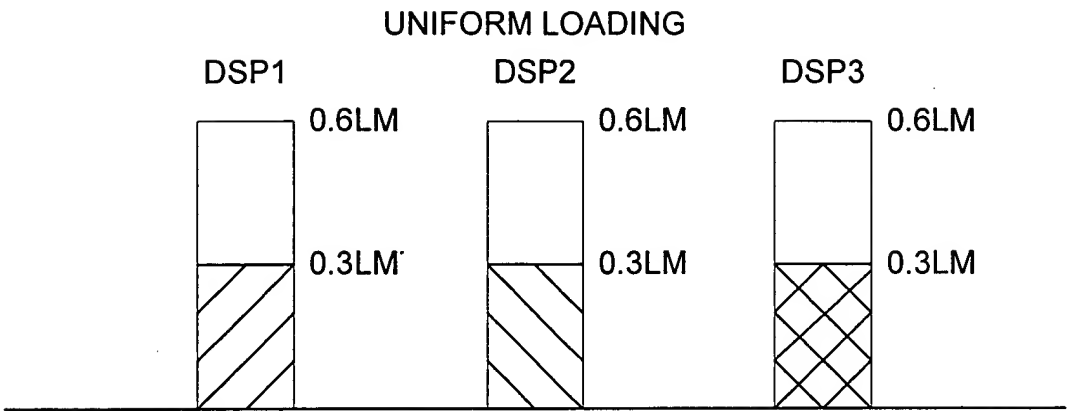



FIG. 5A

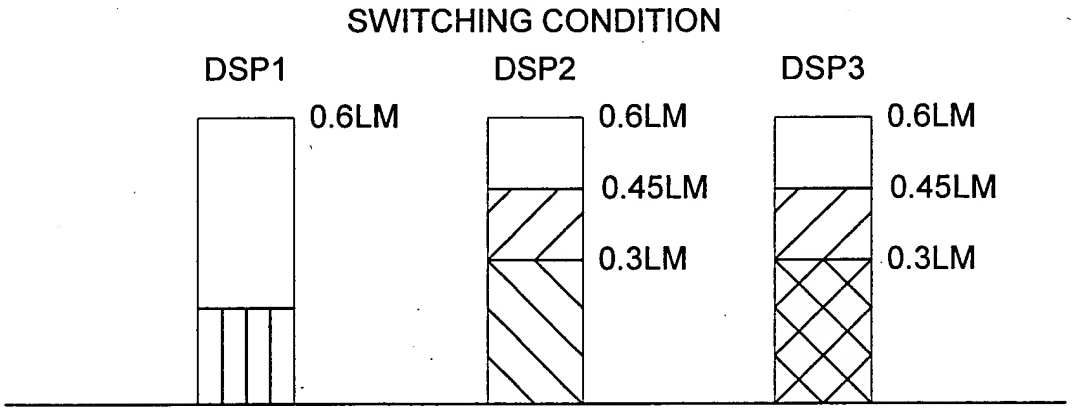



FIG. 5B

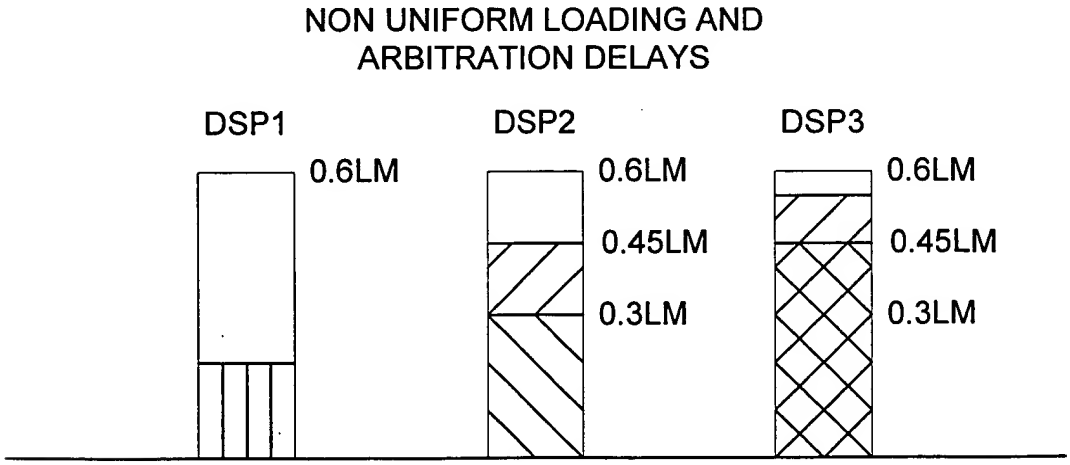



FIG. 5C

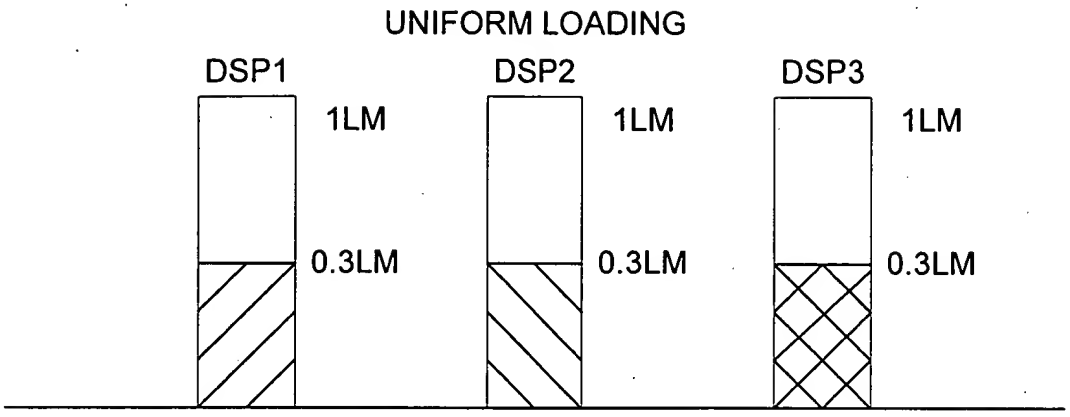



FIG. 6A

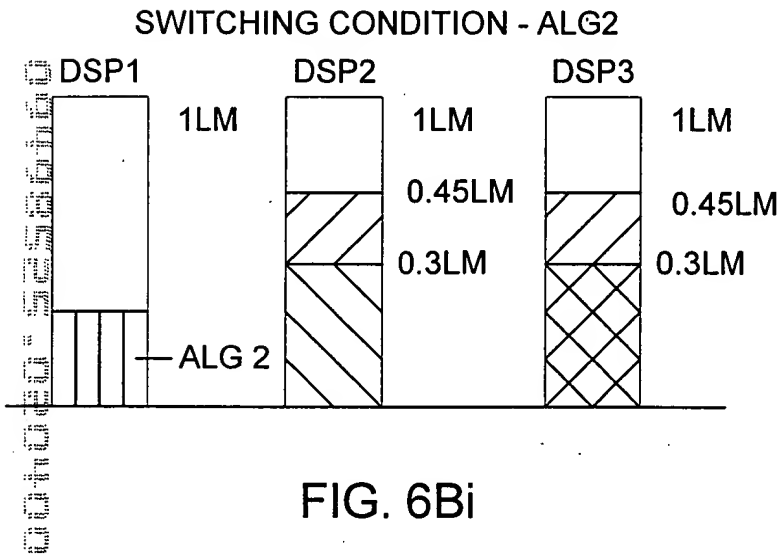



FIG. 6Bi

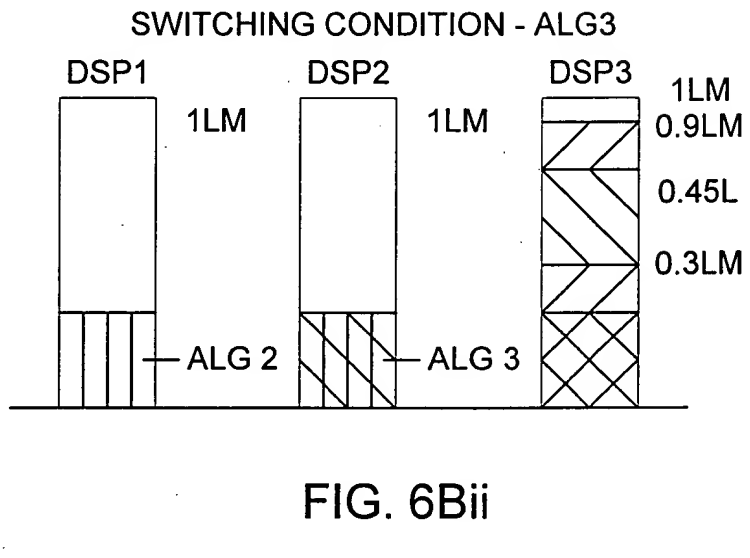



FIG. 6Bii

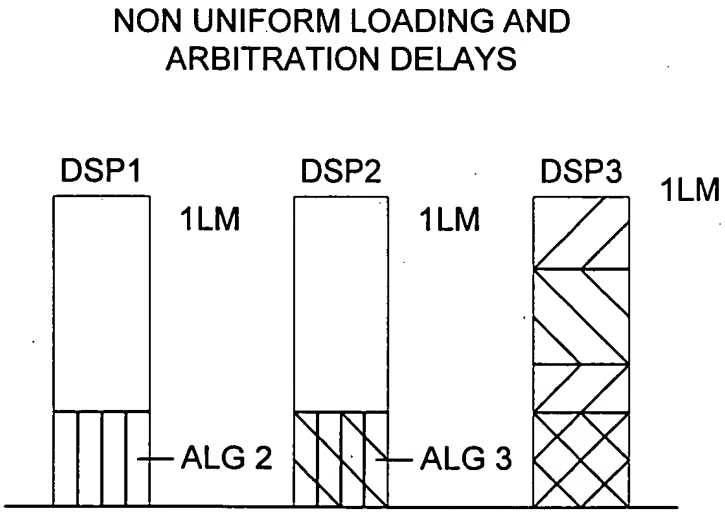
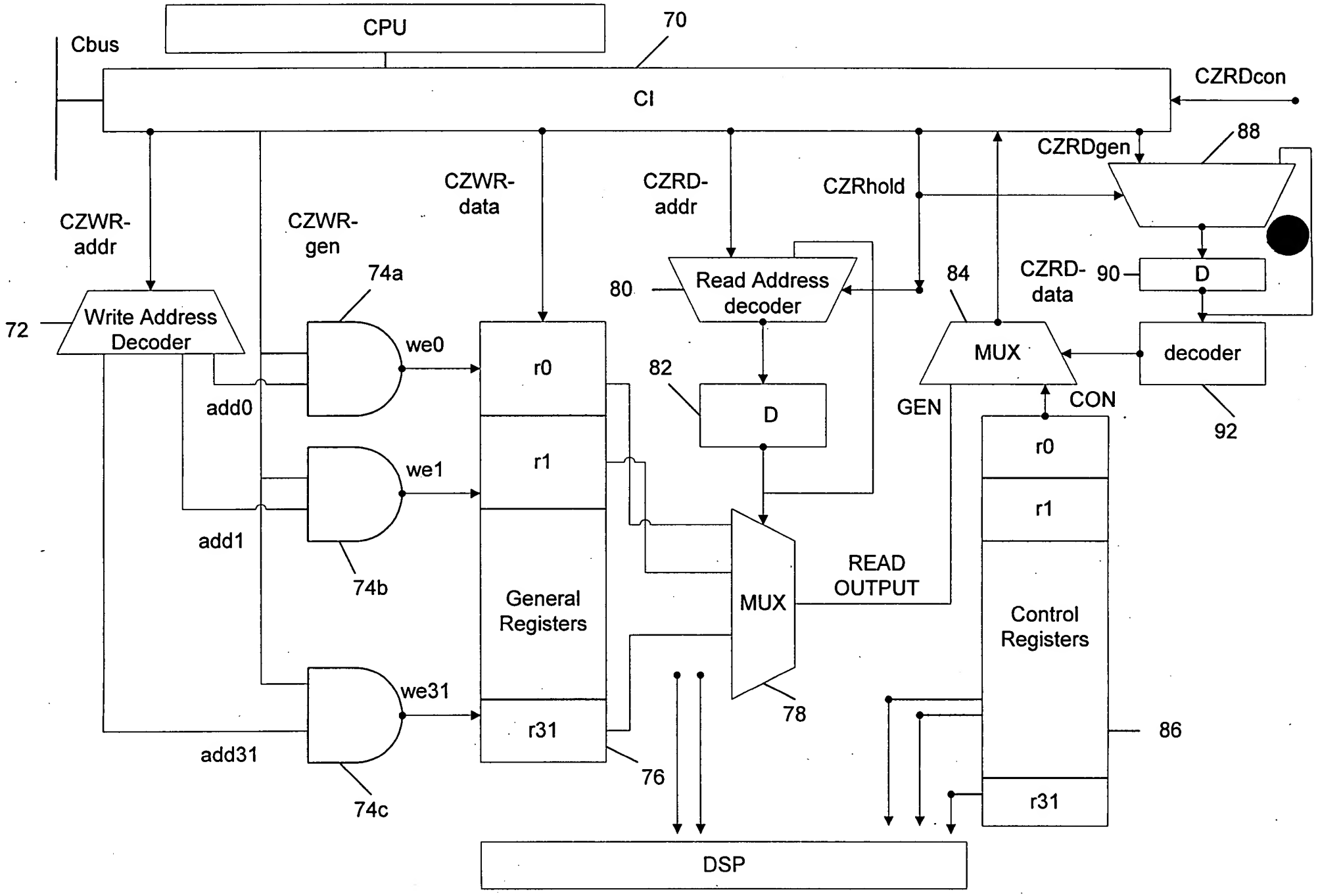



FIG. 6C

FIG. 7A


CPU
70
Cbus
CI
CZRDcon
88
CZRDgen
CZWR-addr
CZWR-gen
CZWR-data
CZRD-addr
CZRhold
74a
80
Read Address decoder
84
CZRD-data
90
D
72
Write Address Decoder
we0
r0
82
MUX
decoder
add0
D
GEN
CON
92
r0
we1
r1
r1
add1
74b
READ OUTPUT
General Registers
MUX
Control Registers
we31
78
86
r31
r31
add31
76
74c
DSP

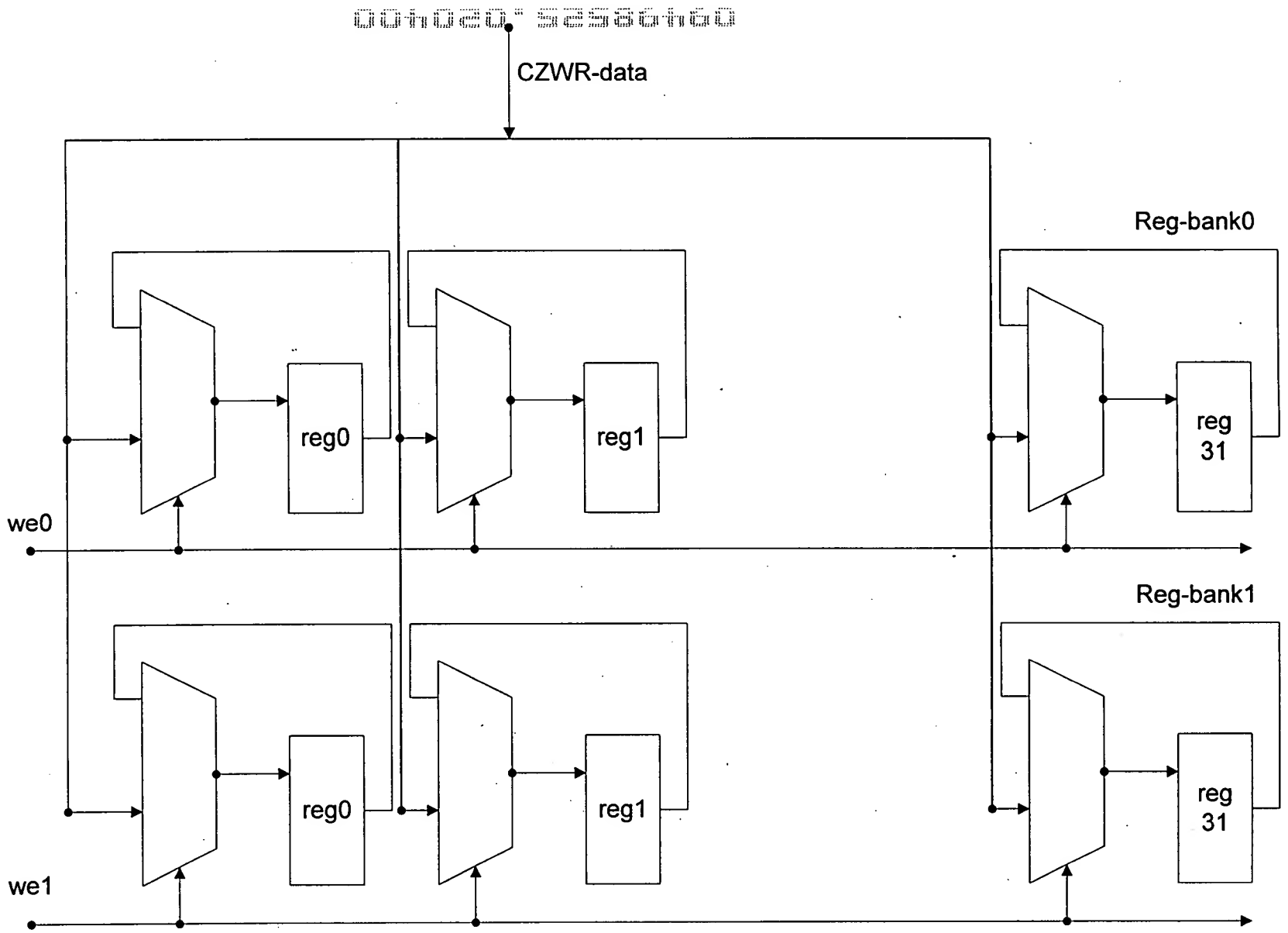

CZWR-data
Reg-bank0
reg0
reg1
reg
31
we0
Reg-bank1
reg0
reg1
reg
31
we1

FIG. 7B

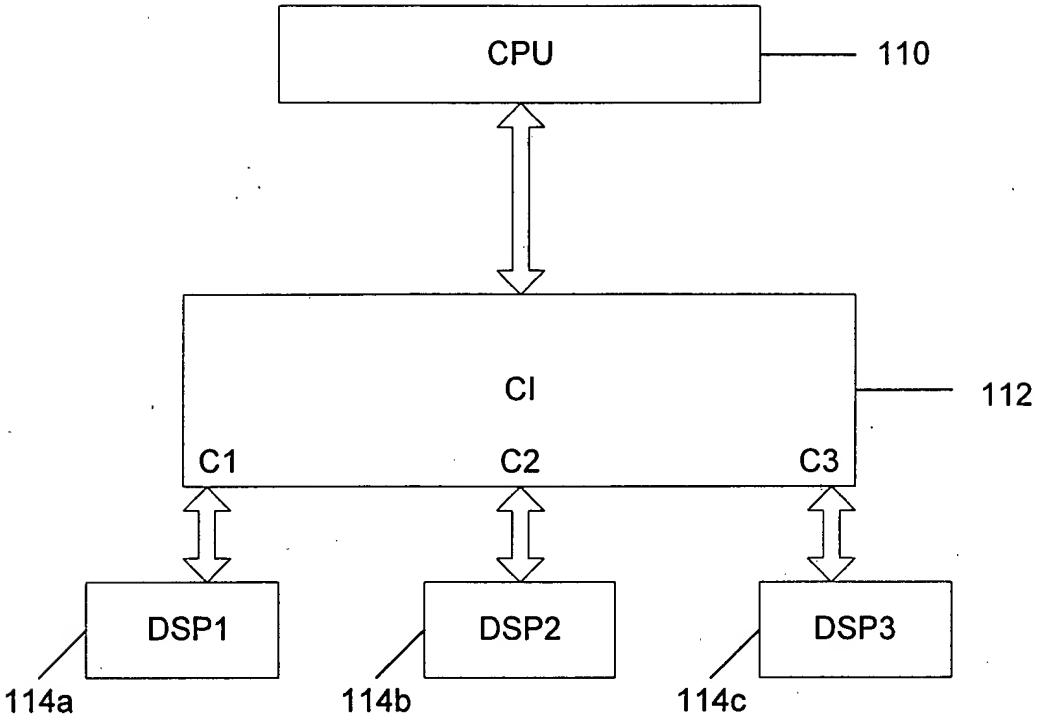

CPU
110
CI
112
C1
C2
C3
DSP1
DSP2
DSP3
114a
114b
114c

FIG. 8A

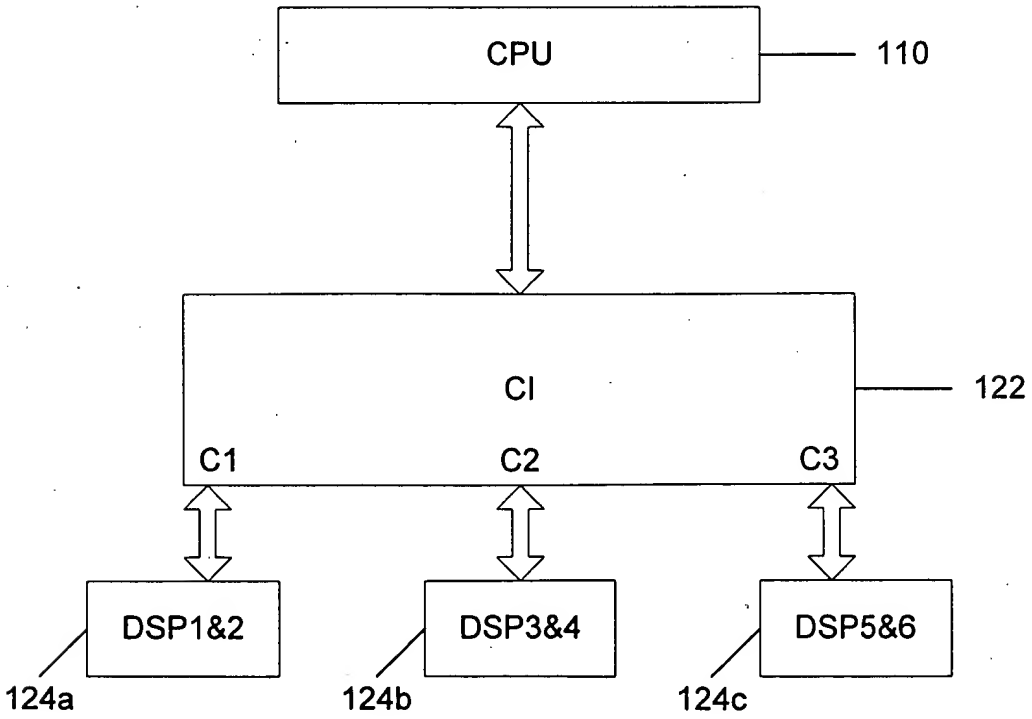

CPU
110
CI
122
C1
C2
C3
DSP1&2
DSP3&4
DSP5&6
124a
124b
124c

FIG. 8B

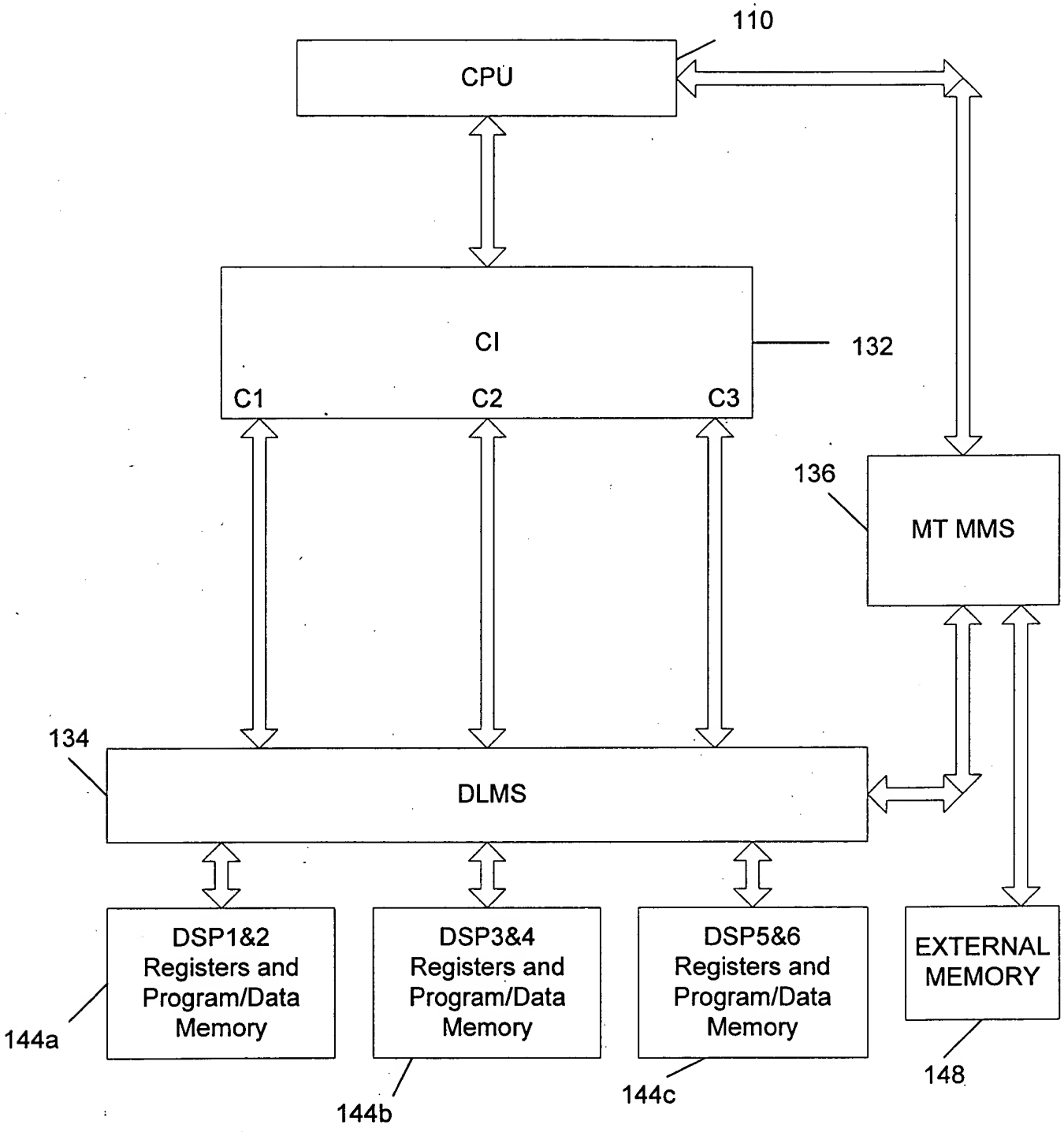

110
CPU
CI
132
C1
C2
C3
136
MT MMS
134
DLMS
DSP1&2 Registers and Program/Data Memory
DSP3&4 Registers and Program/Data Memory
DSP5&6 Registers and Program/Data Memory
EXTERNAL MEMORY
144a
144b
144c
148

FIG. 9A

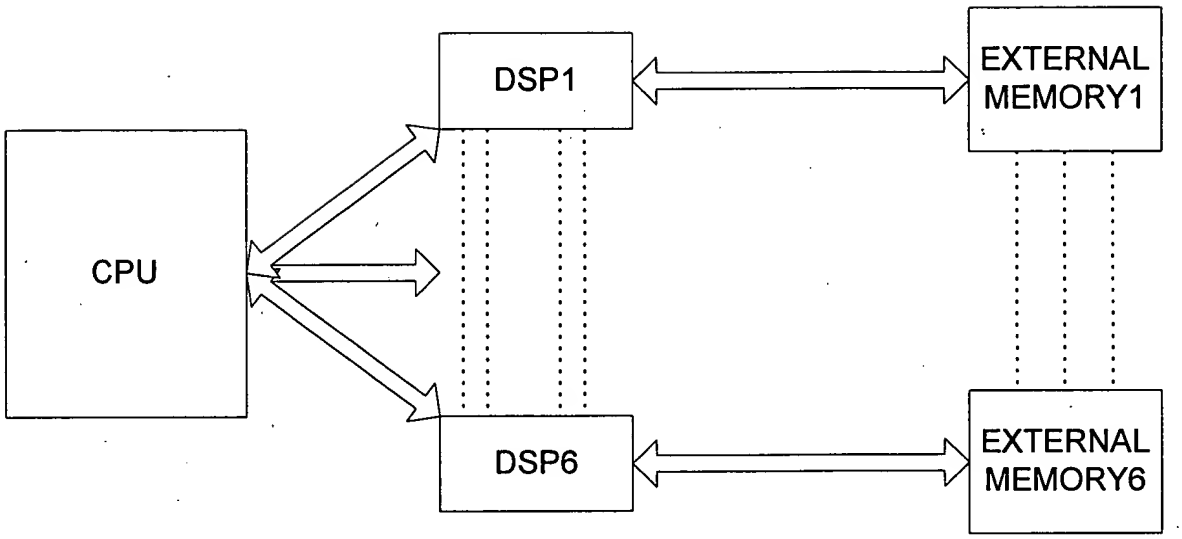



FIG. 9B

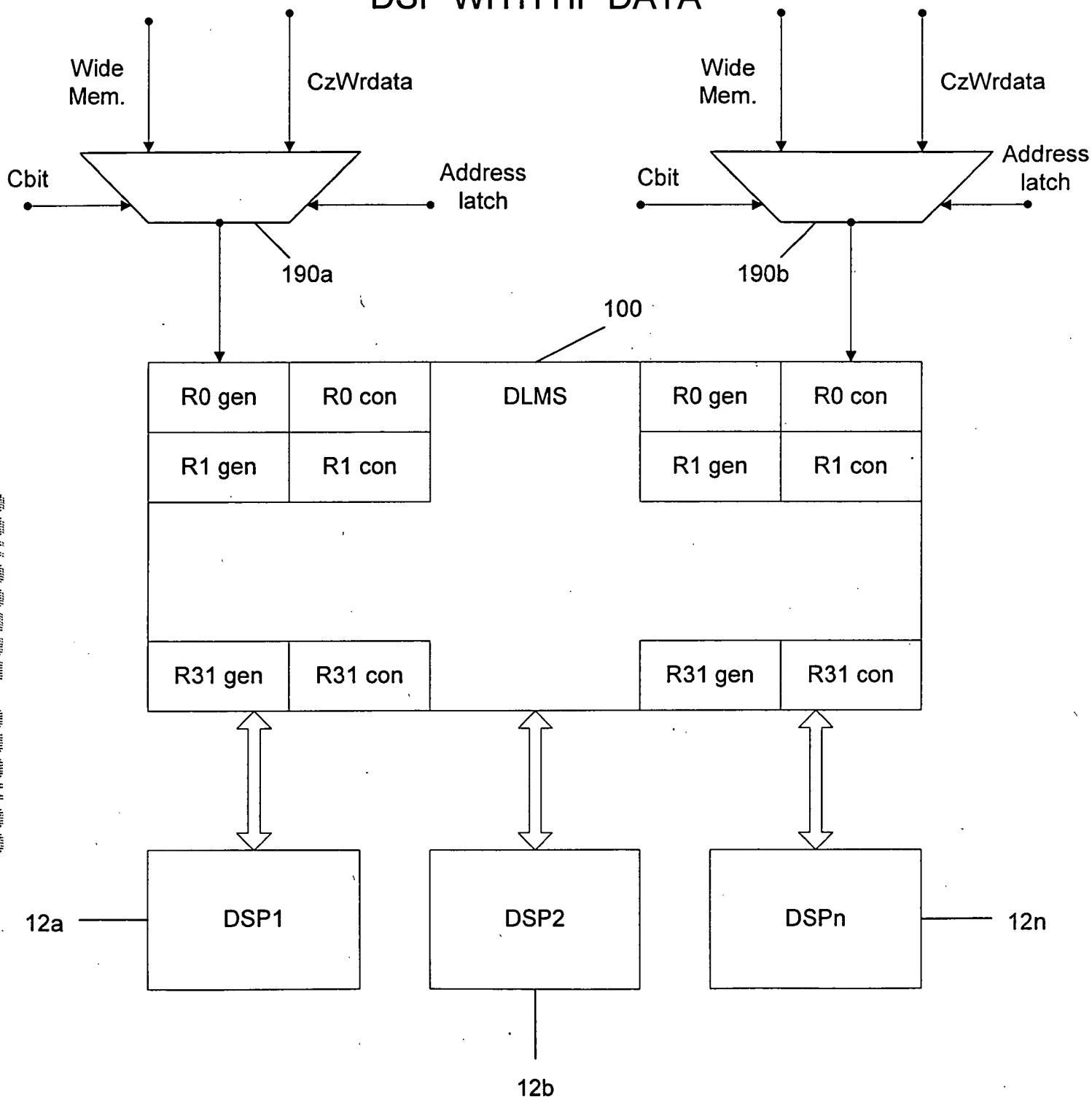

MT MMS LOADING
DSP WITH HF DATA
Wide Mem.
CzWrdata
Cbit
Address latch
190a
Wide Mem.
CzWrdata
Cbit
Address latch
190b
100
R0 gen
R0 con
DLMS
R0 gen
R0 con
R1 gen
R1 con
R1 gen
R1 con
R31 gen
R31 con
R31 gen
R31 con
12a
DSP1
DSP2
DSPn
12n
12b

FIG. 10

# 2 MAC CLUSTER

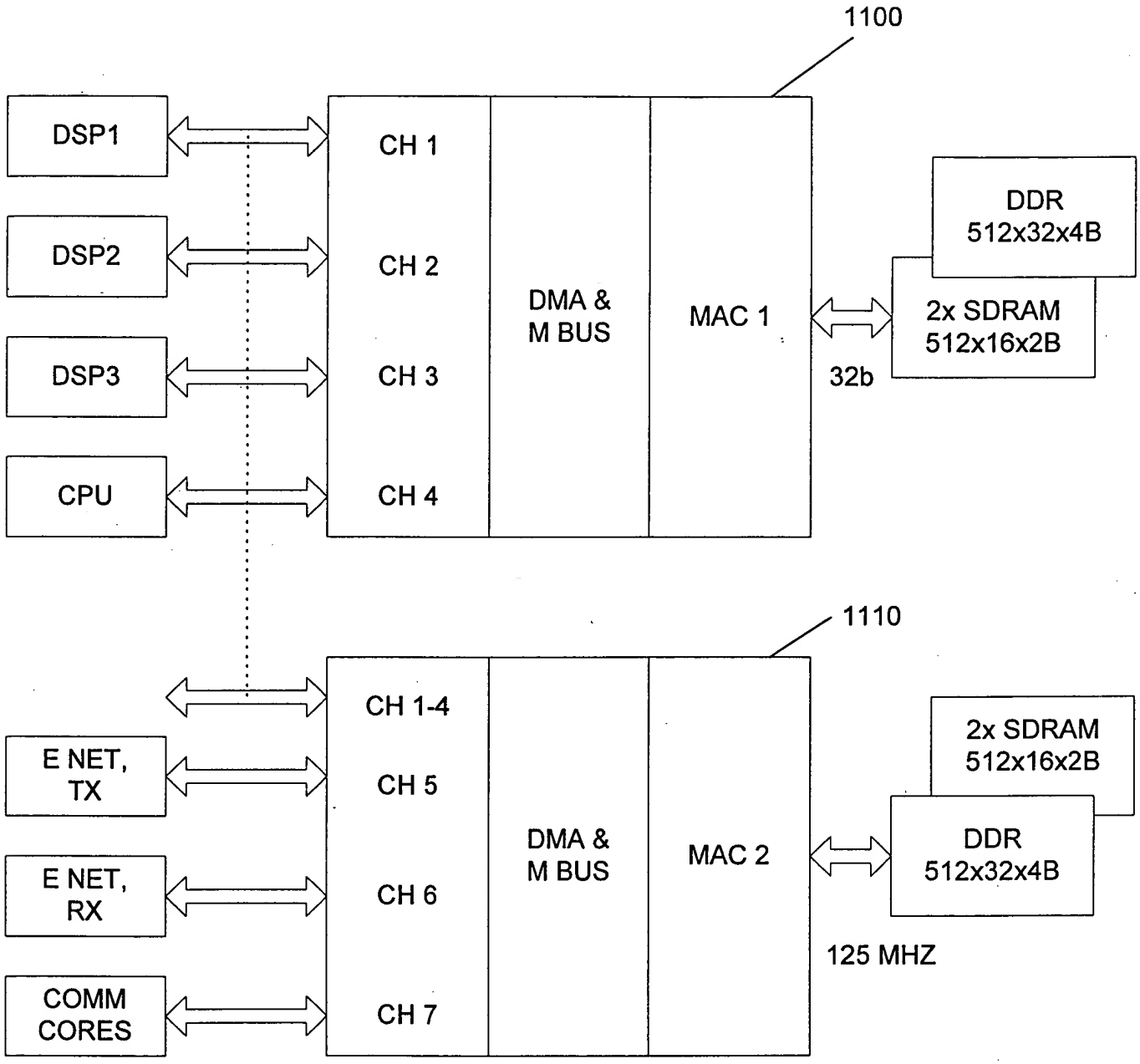



FIG. 11

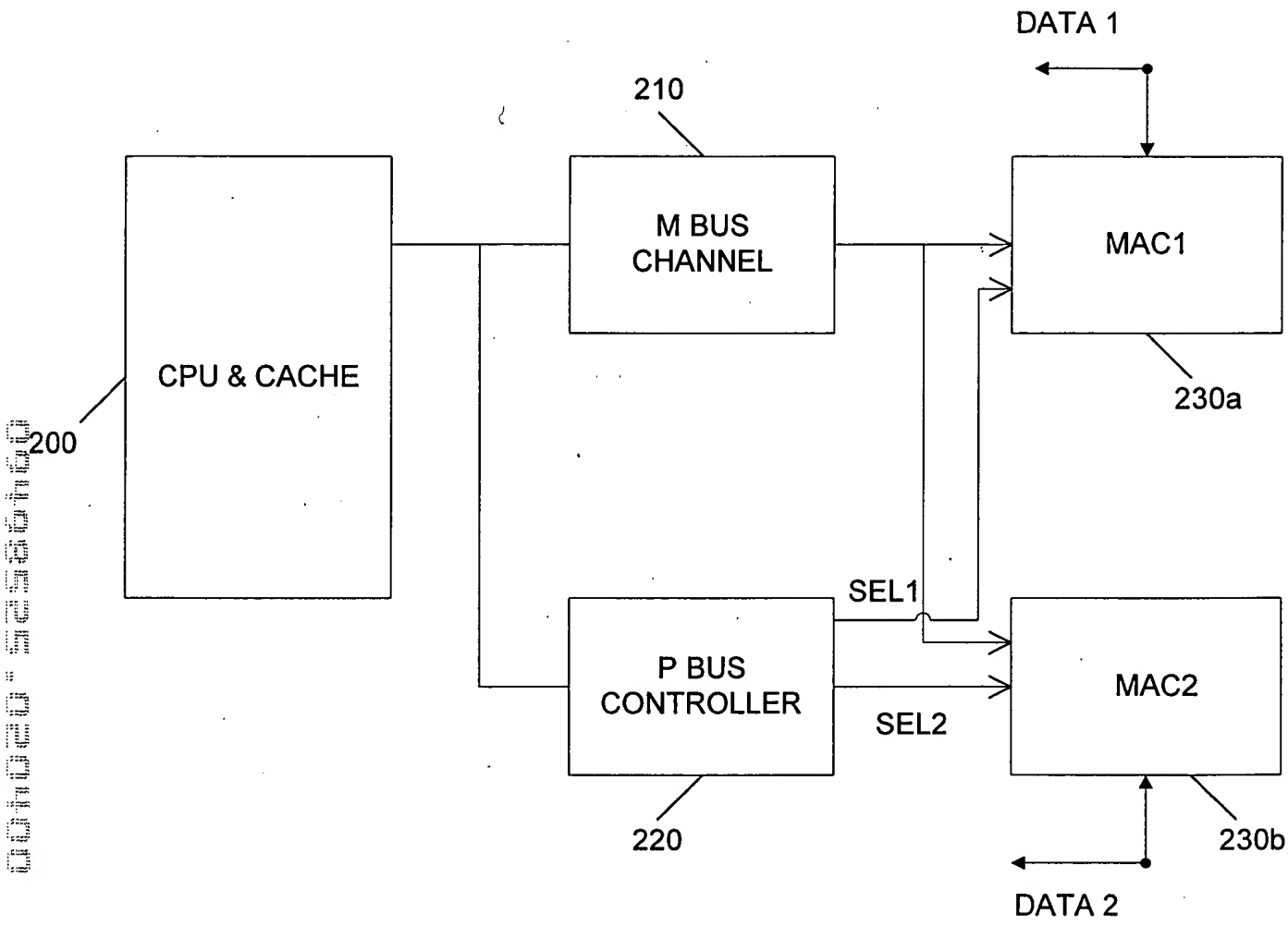

DATA 1
210
M BUS
CHANNEL
MAC1
CPU & CACHE
230a
200
SEL1
P BUS
CONTROLLER
MAC2
SEL2
220
230b
DATA 2

FIG. 12

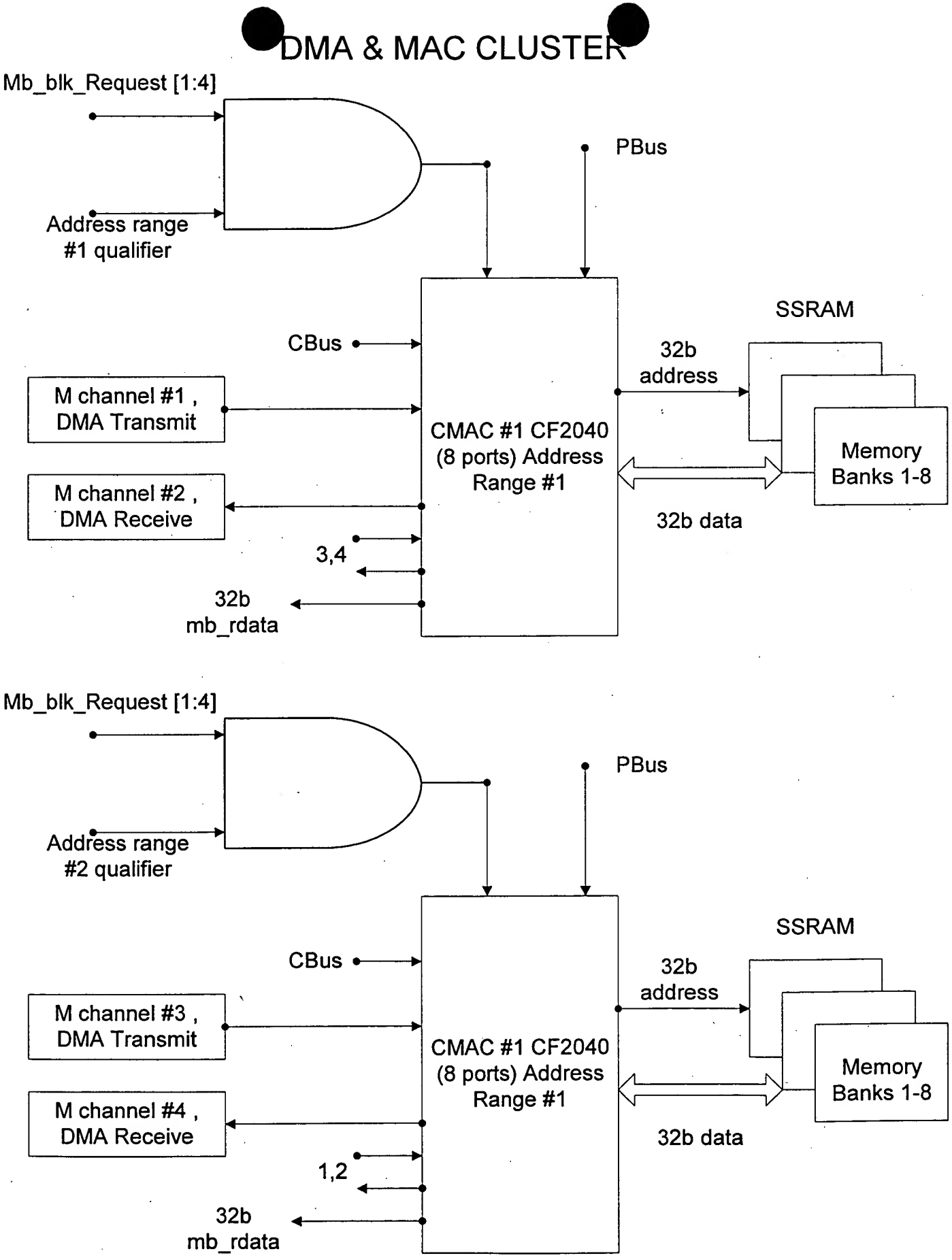

DMA & MAC CLUSTER
Mb_blk_Request [1:4]
Address range
#1 qualifier
PBus
SSRAM
CBus
32b
address
M channel #1 ,
DMA Transmit
CMAC #1 CF2040
(8 ports) Address
Range #1
Memory
Banks 1-8
M channel #2 ,
DMA Receive
32b data
3,4
32b
mb_rdata
Mb_blk_Request [1:4]
Address range
#2 qualifier
PBus
SSRAM
CBus
32b
address
M channel #3 ,
DMA Transmit
CMAC #1 CF2040
(8 ports) Address
Range #1
Memory
Banks 1-8
M channel #4 ,
DMA Receive
32b data
1,2
32b
mb_rdata

FIG. 13

# MULTIPLEXING THE DATA BUS TO INDIVIDUAL CHANNELS

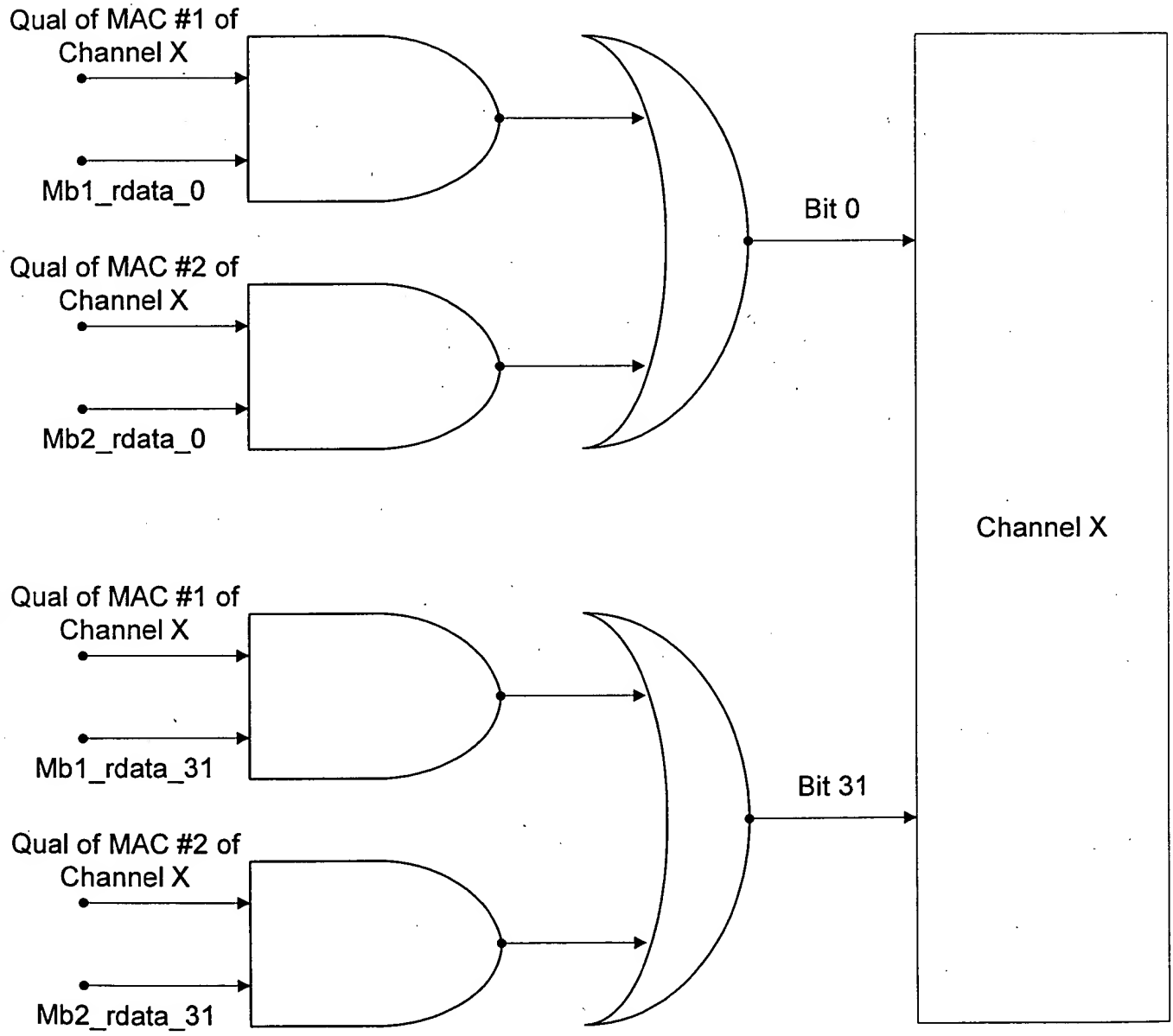
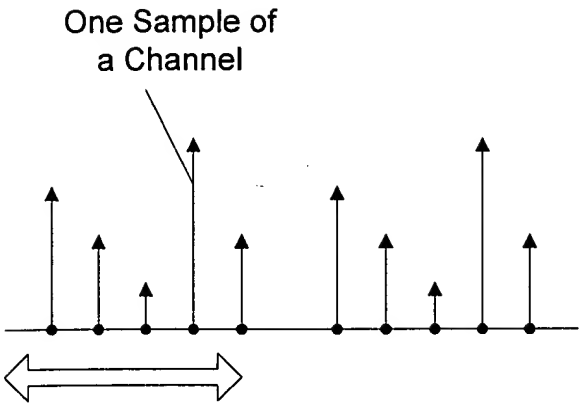



FIG. 14

RE TIME LOAD MANAGEMENT



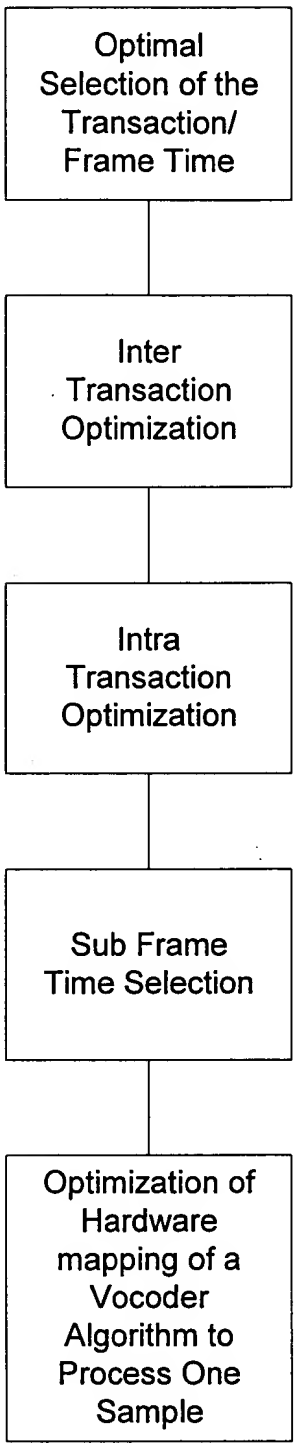




FIG. 15

# DLMS PARALLEL WORD TRANSFER

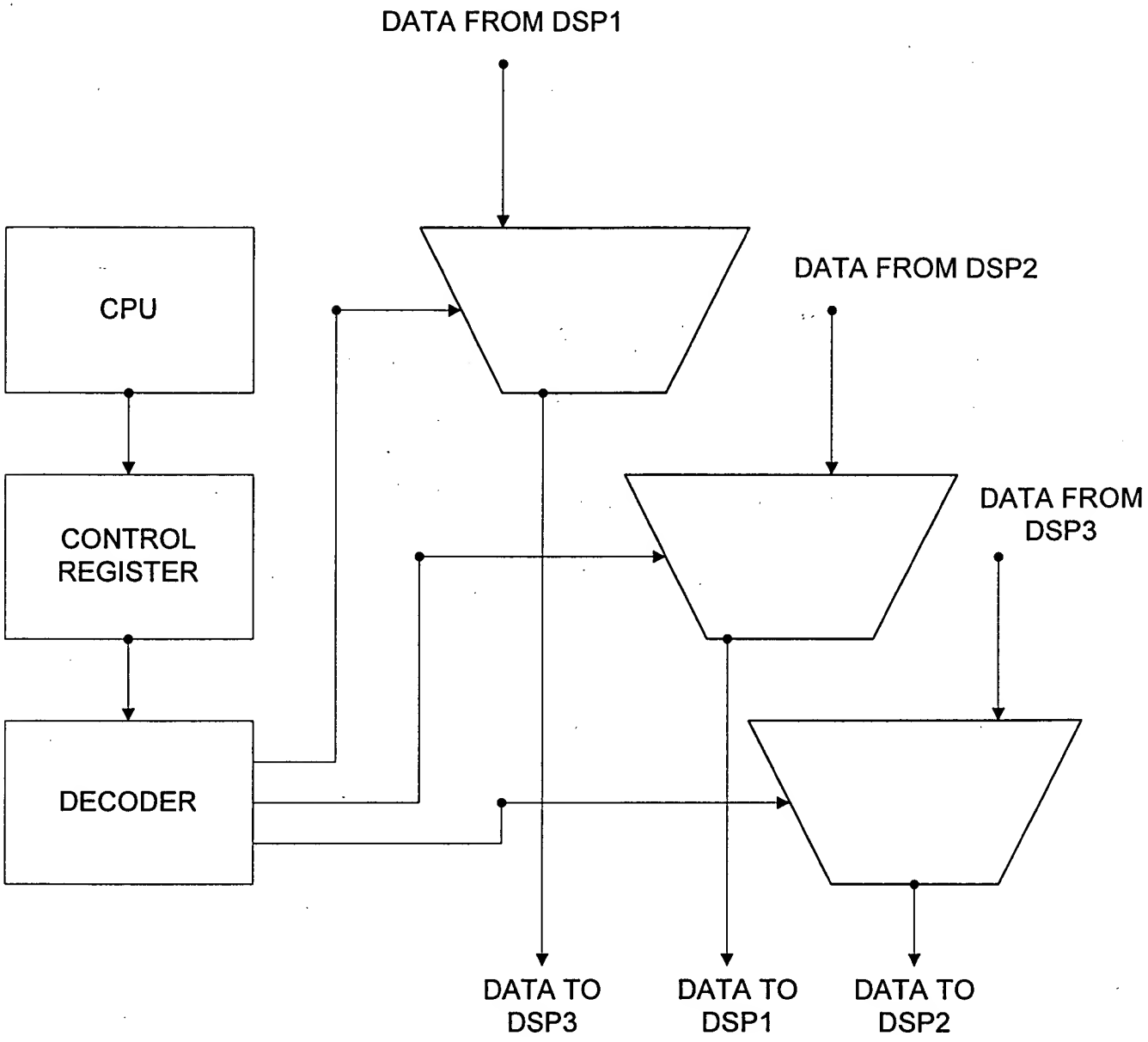



FIG. 16

PE ARRAY

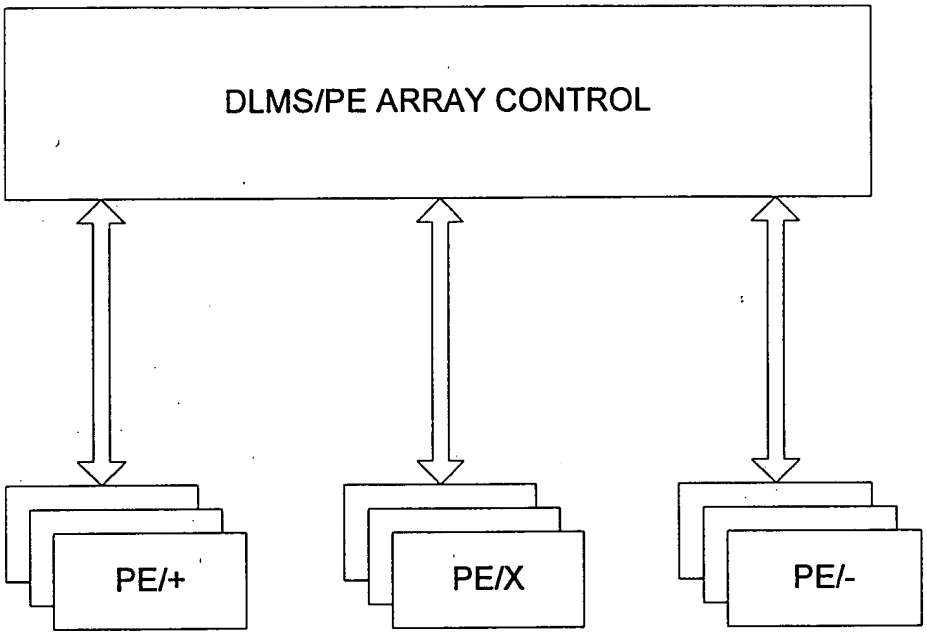



FIG. 17

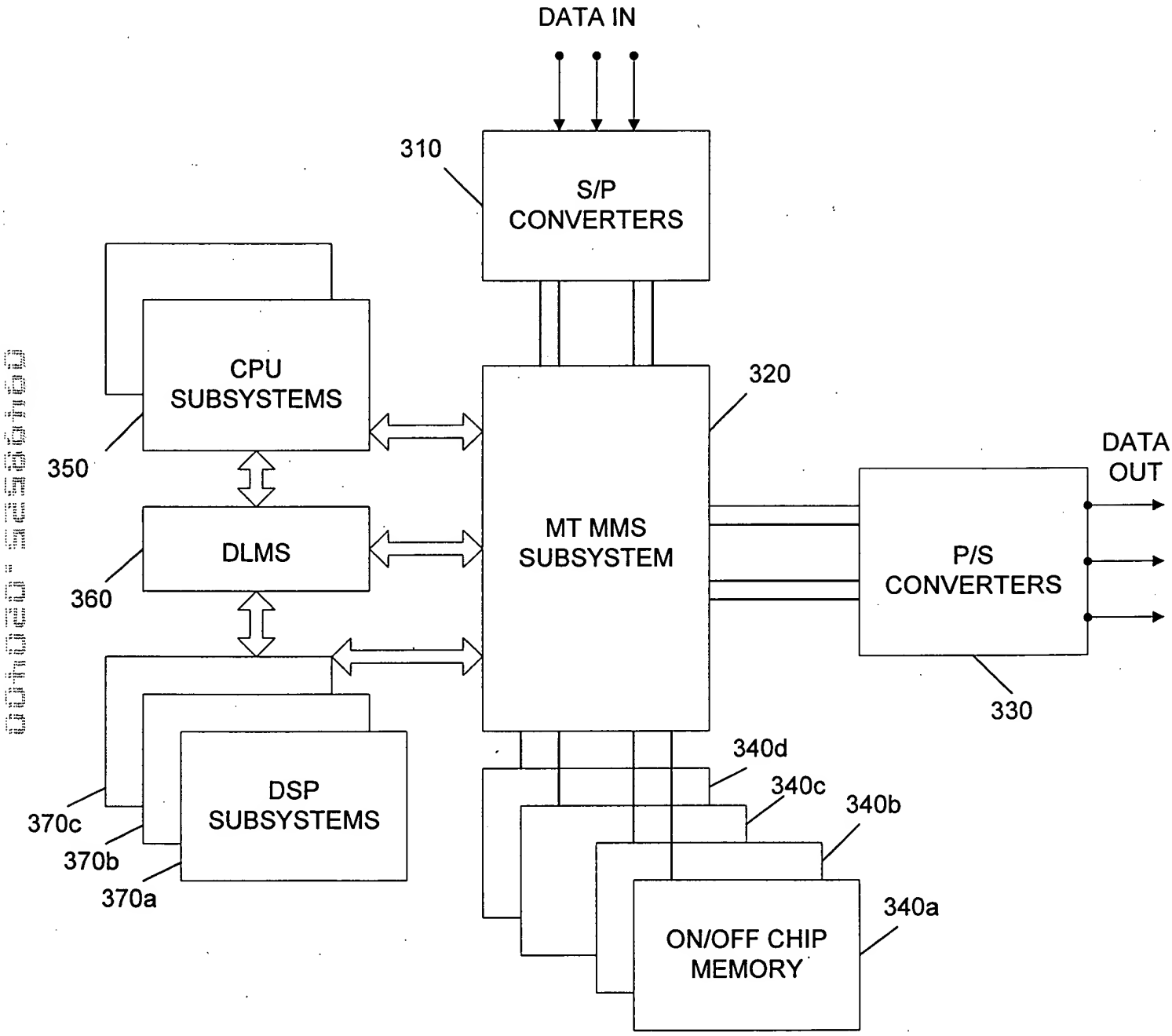

DATA IN
310
S/P
CONVERTERS
CPU
SUBSYSTEMS
350
320
DLMS
360
MT MMS
SUBSYSTEM
DATA
OUT
P/S
CONVERTERS
330
340d
340c
340b
DSP
SUBSYSTEMS
370c
370b
370a
ON/OFF CHIP
MEMORY
340a

FIG. 18A

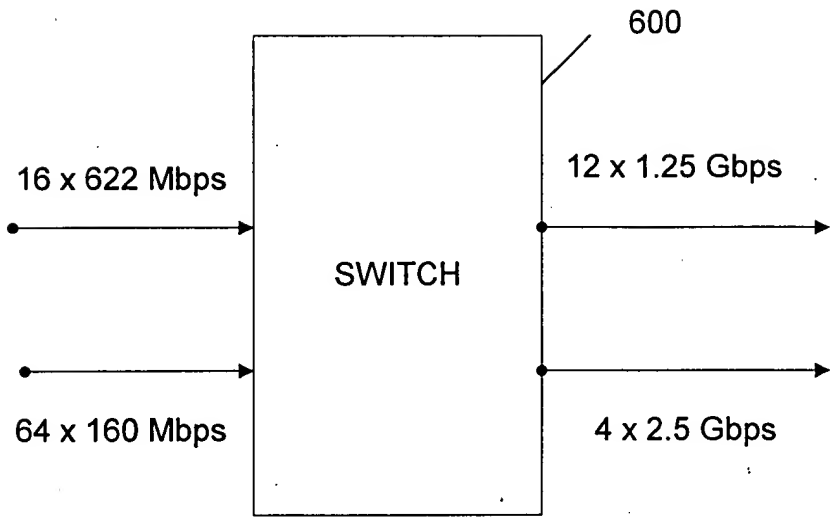



FIG. 18B

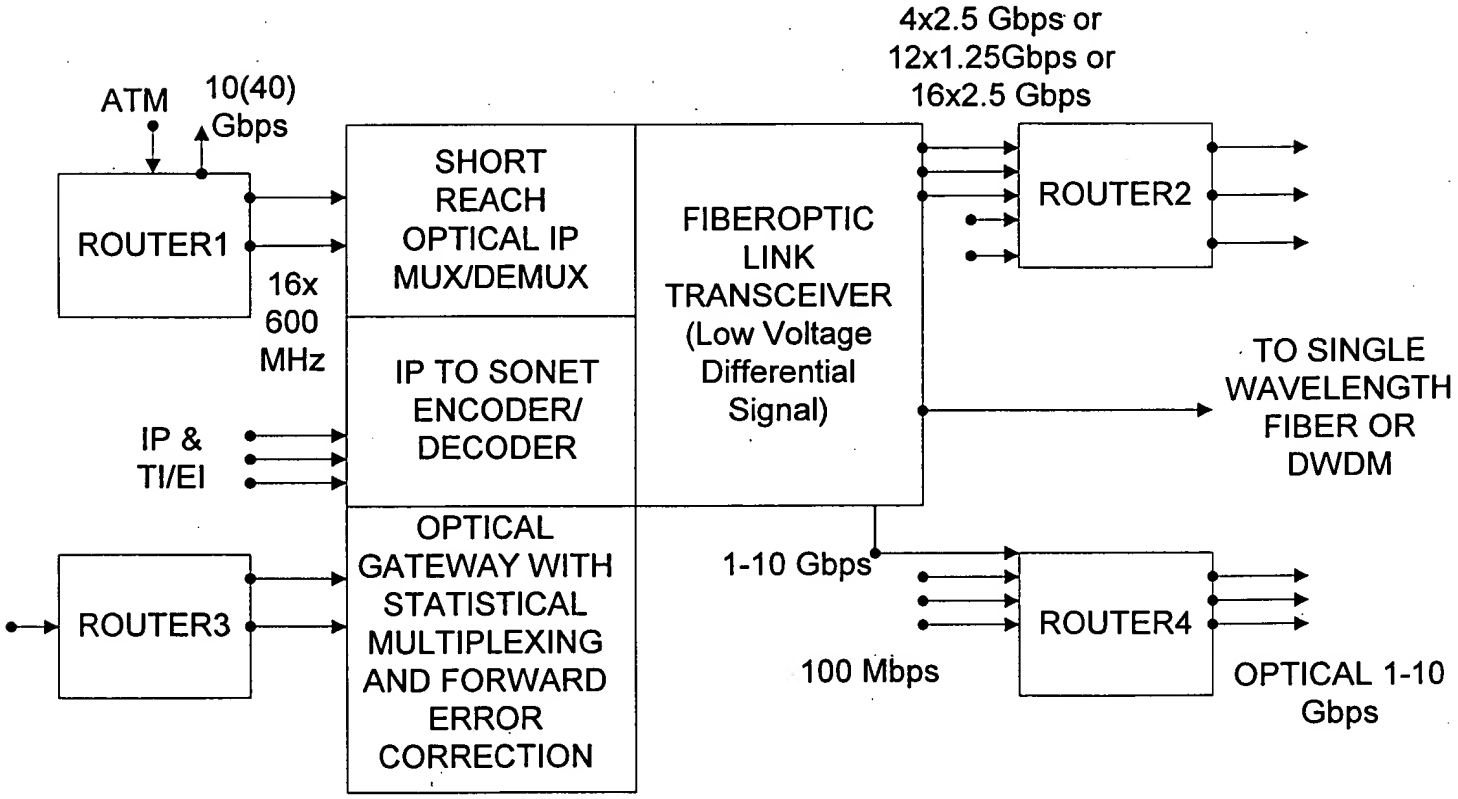



FIG. 18C